IN THE SPECIFICATION:

Please replace the paragraph at page 4, lns. 7-22 with the following amended paragraph:

As shown in Fig. 3, a pixel structure of the active sensor that is mostly adopted is a type that is composed of three N channel transistors and one photo diode, thereby forming one pixel 308. A P channel side terminal of a photo diode 304 is connected to a power source standard line 312, and an N channel side terminal of the photo diode 304 is connected to a gate terminal of an amplifying transistor 306. A drain terminal and a source terminal of the amplifying transistor 306 are connected to a power source line 309 and to a drain terminal of a switching transistor 301, respectively. A gate terminal of the switching transistor 301 is connected to a gate signal line 302 while a source terminal thereof is connected to a signal output line 303. A gate terminal of a resetting transistor 307 is connected to a reset signal line 306. A source terminal and a drain terminal of the resetting transistor [[306]] 307 are connected to the power source line 309 and a gate terminal of the amplifying transistor 306, respectively.

Please replace the paragraph at page 5, ln. 7 - page 6, ln. 7 with the following amended paragraph:

The resetting transistor 307 is first made into a conductive state. Because the P channel side terminal of the photo diode 304 is connected to the power source standard line 312, whereby the photo diode 304 becomes a state in which the N channel side terminal is electrically connected to the power source line 309, an inverted bias voltage is applied to the photo diode 304. Hereinafter, the operation of charging the N channel side terminal of the photo diode 304 until its electric potential is equivalent to the electric potential of the power source line 309 will be referred as "reset". Thereafter, the resetting transistor 307 is made into a non-conductive state. When light is being

irradiated to the photo diode 304, an electric charge is generated due to a photoelectric conversion. Therefore, as time elapses, the electric potential of the N channel side terminal of the photo diode 304, which has been charged up to the electric potential of the power source line 309, gradually becomes smaller because of an electric charge that was generated by the light. Then after a fixed period of time has passed, the switching transistor 301 is made into a conductive state, whereby a signal is ~~outputted~~ output to the signal output line 303 through the amplifying transistor 306. However, at the time the signal is being ~~outputted~~ output, an electric potential is applied to the bias signal line 310 to cause a current to flow in the biasing transistor 311. Therefore, the amplifying transistor 306 and the biasing transistor 311 operate as the so-called source follower circuits.

Please replace the paragraph at page 7, ln. 21 - page 8, ln. 6 with the following amended paragraph:

Therefore, in Fig. 3, if the electric potential of the N channel side terminal of the photo diode 304 is Vpd, the electric potential of the bias signal line 310, that is, the bias electric potential is Vb, the electric potential of the signal output line 303 is Vout, and the electric potential of the power source standard line 312 and the bias side power source line 313 is 0V, then the relationship becomes Vout = Vpd – Vb. Accordingly, when the electric potential Vpd of the N channel side terminal of the photo diode 304 changes, then Vout also changes. As a result, the change of the Vpd can be ~~outputted~~ output as a signal and the light intensity can thus be read.

Please replace the paragraphs at page 17, ln. 21 - page 18, ln. 22 with the following amended paragraphs:

According to the present invention, in a source follower circuit that employs an N channel transistor, prior to outputting a signal therefrom, an output electric potential (electric potential of a load capacitance) is lowered once (in the case of a source follower circuit employing a P channel transistor, the output electric potential is raised). Hereinafter, the process of lowering the output electric potential (electric potential of the load capacitance) of the source follower circuit (in the case where a P channel is employed, increasing the electric potential thereof) is referred to as "pre-discharge", and a period during which the pre-discharge is performed is referred to as "pre-discharge period". In the present invention, an actual signal is ~~outputted~~ output after a pre-discharge.

Conventionally, in a source follower circuit employing an N channel transistor, an electric charge of the load capacitance was discharged through a biasing transistor when Vout > Vin – Vb in the initial state. However, in the present invention, the electric potential of the load capacitance is lowered once to thereby make the source follower circuit in a state where Vout < Vin –Vb. This operation is the pre-discharge. Thereafter, the actual signal is ~~outputted~~ output. Since the follower circuit is already in the state where Vout < Vin – Vb at the time of outputting the actual signal, the signal is ~~outputted~~ output to the load capacitance through an amplifying transistor. Therefore, the signal writing-in time does not become long.

Please replace the paragraph at page 35, lns. 18-22 with the following amended paragraph:

An actual signal is ~~outputted~~ output after the pre-discharge. In that case, since the source follower circuit is in the Vout < Vin – Vb state, a large electric current flows to the amplifying transistor 1101 as the voltage between the gate and the source thereof is large. Consequently, a signal writing-in can be done in a short time.

Please replace the paragraph at page 42, ln. 20 - page 43, ln. 1 with the following amended paragraph:

An actual signal is ~~outputted~~ output after the pre-discharge. In that case, since the source follower circuit is in the Vout < Vin – Vb state, a large electric current flows to the amplifying transistor 1801 because the electric potential between the gate and the source thereof is large. Consequently, the signal writing-in can be done in a short time.

Please replace the paragraph at page 45, ln. 3 - page 46, ln. 10 with the following amended paragraph:

An embodiment of a case in which pre-discharge is performed by employing an electric discharging transistor in an area sensor that has pixels arranged two-dimensional therein and incorporated with driver circuits in the periphery thereof will be explained next. The entire circuit configuration is illustrated in Fig. 20. First, there is provided a pixel arrangement portion 2005 having pixels arranged two-dimensional therein. Driver circuits for driving a gate signal line and a reset signal line of each of the pixels is provided on the left and right sides of the pixel arrangement portion 2005. In Fig. 20, a gate signal line driver circuit 2006 is provided on the left side and a reset signal line driver circuit 2007 is provided on the right side. Driver circuits such as a signal processing circuit are arranged above the pixel arrangement portion 2005. A biasing circuit 2003 is arranged above the pixel arrangement portion 2005 in Fig. 20. The biasing circuit 2003 and the amplifying transistors of the respective pixels form the source follower circuit. A sample hold and signal processing circuit 2002 are arranged above the biasing circuit 2003. Circuits for maintaining signals for a time, for performing analog/digital conversion, or for reducing noise are arranged here. A signal output line driver circuit 2001 is arranged above the sample hold and signal processing

circuit 2002. The signal output line driver circuit 2001 outputs signals for outputting, in sequence, the signals that have been temporarily preserved. Then, before the signals are ~~outputted~~ output to the outside, a final output amplifying circuit 2004 is arranged thereto. Before the signals, which are sequentially ~~outputted~~ output hereto by the sample hold and the signal processing circuit 2002 and the signal output line driver circuit 2001, are ~~outputted~~ output to the outside, the signals are amplified by the final output amplifying circuit 2004. Therefore, although unnecessary when the signals are not amplified, in practice it is often provided.

Please replace the paragraph at page 51, ln. 18 - page 53, ln. 5 with the following amended paragraph:

Next, the circuit configuration of a jth row peripheral portion circuit 2009 taken as an exemplary row of circuits from inside the biasing circuit 2003 and the sample hold and signal processing circuit 2002 is shown in Fig. 23. A biasing transistor 2311 is arranged in the biasing circuit 2003. The polarity thereof is the same as the polarity of the amplifying transistor of the respective pixels. Therefore, if the amplifying transistor of the pixel is the N channel type, the biasing transistor is also the N channel type. In Fig. 23, the biasing transistor 2311 is the N channel type. A gate terminal of the biasing transistor 2311 is connected to a biasing signal line 2310, and a source terminal and a drain terminal thereof are connected to a jth row signal output line 2303 and a power source standard line 2312 (when the biasing transistor is the P channel type, the power source line is used in place of the power source standard line). The biasing transistor 2311 and the amplifying transistors of the respective pixels, operates as the source follower circuit. A gate terminal of a transferring transistor 2313 is connected to a transfer signal line 2314, and a source terminal and a drain terminal thereof are connected to a jth row signal output line 2303 and a load

capacitance 2315. The transferring transistor is operated when transferring the electric potential of the signal output line 2303 to the load capacitance 2315. Therefore, a P channel type transferring transistor may be added and connected in a row to an N channel type transferring transistor 2314. The load capacitance 2315 is connected to the transferring transistor 2313 and the power source standard line 2312. The role of the load capacitance 2315 is to temporarily accumulate therein the signals ~~outputted~~ output from the signal output line 2303. A gate terminal of an electric discharging transistor 2316 is connected to a pre-discharge signal line 2317, and a source terminal and a drain terminal thereof are connected to the load capacitance 2315 and the power source standard line 2312. Prior to inputting the electric potential of the signal output line 2303 to the load capacitance 2315, the electric discharging transistor 2316 operates to discharge the electric charges that have temporarily accumulated in the load capacitance 2315.

Please replace the paragraph at page 53, ln. 8 - page 54, ln. 12 with the following amended paragraph:

A final selecting transistor 2319 is connected between the load capacitance 2315 and a final output line 2320. A source terminal and a drain terminal of the final selecting transistor 2319 are connected to the load capacitance 2315 and the final output line 2320, and a gate terminal thereof is connected to a jth row final selecting line 2318. The final selecting line will be scanned from the first row in sequence. Then the jth row final selecting line 2318 is selected, and when the final selecting transistor 2319 is turned into conductive, the electric potential of the load capacitance 2315 and that of the final output line 2320 become equivalent. As a result, the signals that have accumulated in the load capacitance 2315 can be ~~outputted~~ output to the final output line 2320. However, if electric charges are accumulated in the final output line 2320 before outputting the

signals to the final output line 2320, the electric potential when outputting the signals to the final output line 2320 will be adversely influenced by those electric charges. Therefore, the electric potential of the final output line 2320 must be initialized to a certain electric potential value before the signals are ~~outputted~~ output to the final output line 2320. In Fig. 23, a final resetting transistor 2322 is arranged between the final output line 2320 and the power source standard line 2312. A gate terminal of the final resetting transistor 2322 is connected to a jth row final resetting line 2321. Prior to selecting the jth row final selecting line 2318, the jth row final resetting line 2321 is selected to thereby initialize the electric potential of the final output line 2320 and that of the power source standard line 2312. Thereafter, the jth row final selecting line 2318 is selected, whereby the signals that have accumulated in the load capacitance 2315 are ~~outputted~~ output to the final output line 2320.

Please replace the paragraph at page 54, ln. 13 - page 55, ln. 13 with the following amended paragraph:

The signals that will be ~~outputted~~ output to the final output line 2320 may be withdrawn to the outside. However, because the signals are faint, the signals are frequently amplified before being withdrawn to the outside.. As a circuit for carrying out the amplification of the signals, the circuit configuration of the final portion circuit 2010 is shown in Fig. 24. There are various kinds of circuits for amplifying the signals, such as an arithmetic amplifier. Any kind of circuit that can amplify the signals may be used. As the most simple circuit configuration, the source follower circuit is shown here. In Fig. 24, the N channel type is illustrated. Signals that are ~~inputted~~ input to the final output amplifying circuit 2004 will be ~~inputted~~ input to a final output line 2402. Signals are ~~outputted~~ output from the first row in sequence from the final output line 2402. The signals are amplified by the final output amplifying circuit 2004 and then ~~outputted~~ output to the outside. The final output

line 2402 is connected to a gate terminal of a final output amplifier-amplifying transistor 2404. A drain terminal of the final output amplifier-amplifying transistor 2404 is connected a power source line 2404, and a source terminal thereof serves as an output terminal. A gate terminal of a final output amplifier-biasing transistor 2403 is connected to a final output amplifying bias signal line 2405, and a source terminal and a drain terminal thereof are connected to a power source standard line 2407 and a source terminal of the final output amplifier-amplifying transistor 2404.

Please replace the paragraphs at page 56, ln. 19 - page 59, ln. 17 with the following amended paragraphs:

A timing chart of a signal will be explained next. The timing chart of the circuit shown in Fig. 20 is illustrated in Fig. 26. The reset signal line is scanned sequentially from the first line. For example, first an (i-1)th line is selected, followed by an ith line, and then an (i+1)th line is selected. A period until the same line is selected again corresponds to a frame period. Similarly, the gate signal line is sequentially scanned from the first line. However, the timing to start scanning the gate signal line is later than the timing to start scanning the reset signal line. For instance, directing the attention to a pixel of the ith line, the ith line reset signal line is selected, and thereafter the ith line gate signal line is selected. When the ith line gate signal line is selected, a signal is ~~outputted~~ output from the pixel of the ith line. A period from the time the pixel is reset until the signal is ~~outputted~~ output becomes an accumulation time. During the accumulation time, electric charges generated by light are being accumulated in the photo diode. The timing to reset and the timing to output a signal are different in each line. Therefore, although the accumulation time of the pixels in all the lines are equivalent, the time that signals are accumulated therein is different.

Next, the timing chart of a signal of Fig. 23 is shown in Fig. 27. Because the operation is repetitious, the time that the ith line gate signal line is selected will be taken as an example and observed. First, after the ith line gate signal line 2102 is selected, the pre-discharge signal line 2317 is selected to thereby make the electric discharging transistor 2316 in conductive. Subsequently, the transfer signal line 2314 is selected, whereby the signal of each of the rows from the ith line pixel is ~~outputted~~ output to the load capacitance 2315 of every row.

After accumulating the signals of all the pixels of the ith line in the load capacitance 2315 of every row, the signals of every row are sequentially ~~outputted~~ output to the final output line 2320. During the period from the time the transfer signal line 2314 has become non-selective to the time the gate signal line is selected, all the rows are scanned by the signal output line driver circuit 2001. First, the final reset line of the first row is selected to thereby make the final resetting transistor 2322 into conductive, whereby the electric potential of the final output line 2320 is initialized to that of the power source standard line 2312. Thereafter, the final selecting line 2318 of the first row is selected and the final selecting transistor 2319 is turned into conductive to thereby output the signal in the load capacitance 2315 of the first row to the final output line 2320. Next, the final reset line of the second row is selected to thereby make the final resetting transistor 2322 into conductive, whereby the electric potential of the final output line 2320 is initialized to that of the power source standard line 2312. Thereafter, the final selecting line 2318 of the second row is selected and the final selecting transistor 2319 is turned into conductive to thereby output the signal in the load capacitance 2315 of the second row to the final output line 2320. The operation is repeated thereafter. Similarly, in the case of the jth line, the final reset line of the jth row is selected to thereby make the final resetting transistor 2322 into conductive, whereby the electric potential of the final output line 2320 is initialized to that of the power source standard line 2312. Thereafter, the final selecting line 2318

of the jth row is selected and the final selecting transistor 2319 is turned into conductive to thereby output the signal in the load capacitance 2315 of the jth row to the final output line 2320. Next, the final reset line of the (j+1)th row is selected and the final resetting transistor 2322 is turned into conductive, whereby the electric potential of the final output line 2320 is initialized to that of the power source standard line 2312. Thereafter, the final selecting line 2318 of the (j+1)th row is selected and the final selecting transistor 2319 is turned into conductive to thereby output the signal in the load capacitance 2315 of the (j+1)th row to the final output line 2320. The same operation is repeated thereafter to sequentially output all the signals to the final output line. During this operation, the bias signal line 2310 is fixed. The signals ~~outputted~~ output to the final output line 2320 are amplified by the final output amplifying circuit 2004 and then ~~outputted~~ output to the outside.

Please replace the paragraph at page 60, lns. 15-20 with the following amended paragraph:

As explained so far, the photoelectric conversion element is often connected to the input terminal of the source follower circuit. However, a switch may be sandwiched therebetween like a photo gate type, or the signal, after it has been processed so that it is a logarithmic value of light density, may be ~~inputted~~ input to the input terminal, like a logarithm conversion type.

Please replace the paragraph at page 61, ln. 15- page 62, ln. 3 with the following amended paragraph:

Next, the timing chart of a signal in Fig. 29 is shown in Fig. 28. Because the operation is repetitious, the case in which the ith line gate signal line is selected will be taken as an example and observed. First, after the ith line gate signal line 2102 is selected, the electric potential of a bias

signal line 2910 and that of a transferring transistor 2913 are raised to thereby perform pre-discharge. Then the electric potential of the bias signal line 2910 is returned to its original value, whereby the signal of each of the rows from the ith line pixels is ~~outputted~~ output to a load capacitance 2915 of every row. The signal of each of the rows is sequentially ~~outputted~~ output to a final output line 2920 after the signals of all the ith line pixels have accumulated in the load capacitance 2915 of every row.

Please replace the paragraph at page 73, lns. 5-11 with the following amended paragraph:

In embodiment 3, the amplifier TFT 270 and the bias TFT 273 are an n-channel TFT, and both of source region side and drain region side have LDD regions 281-282 and 284-285 ~~to 284~~. Note that the LDD regions 281-282 and 284-285 ~~to 284~~ do not overlap with the gate electrodes 212 and 215 through the gate insulating film 211. The above constitution of the amplifier TFT 270 and the bias TFT 273 can reduce the hot carrier injection as much as possible.